Semiconductor Electronics - Extrinsic Semiconductors

(a)Doping: The process of mixing impurities of other elements in pure semiconductors is known as doping.

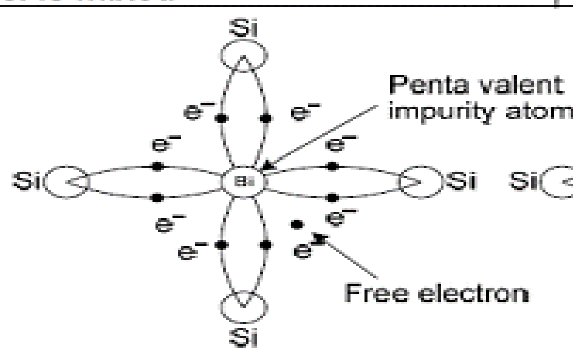
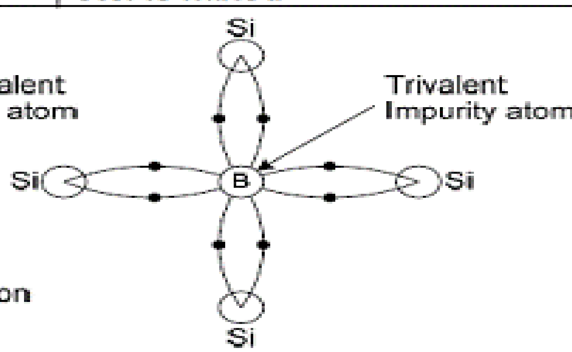
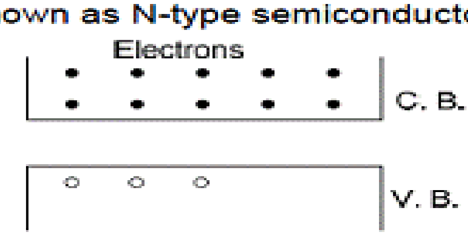
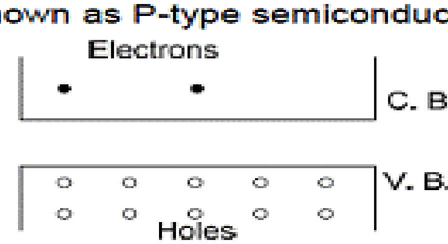
(b)Extrinsic semiconductors: the semiconductors, in which trivalent and pentavalent elements are mixed as impurities, are known as extrinsic semiconductors.

(c) The extrinsic semiconductors are of two types

(i) N-type semiconductors

(ii) P-type semiconductors.

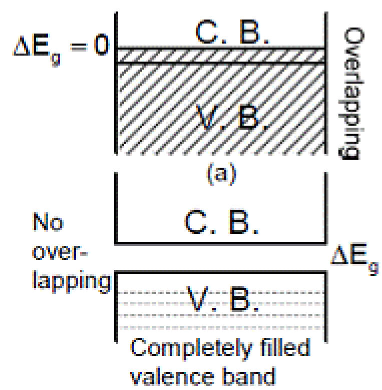
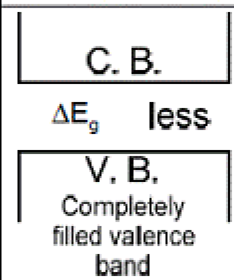
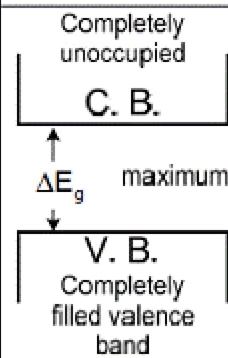
d) Difference between N-type and P-type semiconductors

S.No.	N-type semiconductors	P-type semiconductors
1.	In these the impurity of some pentavalent element like P, As, Sb, Bi, etc. is mixed	In these, the impurity of some trivalent element like b, Al, In, Ga etc. is mixed
2.		
3.	In these the impurity atom donates one electrons, hence these are known as donor type semiconductors	In these, the impurity atom can accept one electron, hence these are known as acceptor type semiconductors.
4.	In these the electrons are majority current carriers and holes are minority current carriers. (i.e. the electron density is more than hole density $n_n >> n_p$)	In these the holes are majority current carriers and electrons are minority current carriers i.e. $n_p >> n_n$
5.	In these there is majority of negative particles (electrons) and hence are known as N-type semiconductors 	In these there is majority of positive particles (cotters) and hence are known as P-type semiconductors. 
6.	In these the donor energy level is close to the conduction band and far away from valence band.	In these the acceptor energy level is close to the valence band and far away from conduction band.

(e) Characterizes Si and Ge at 300 K

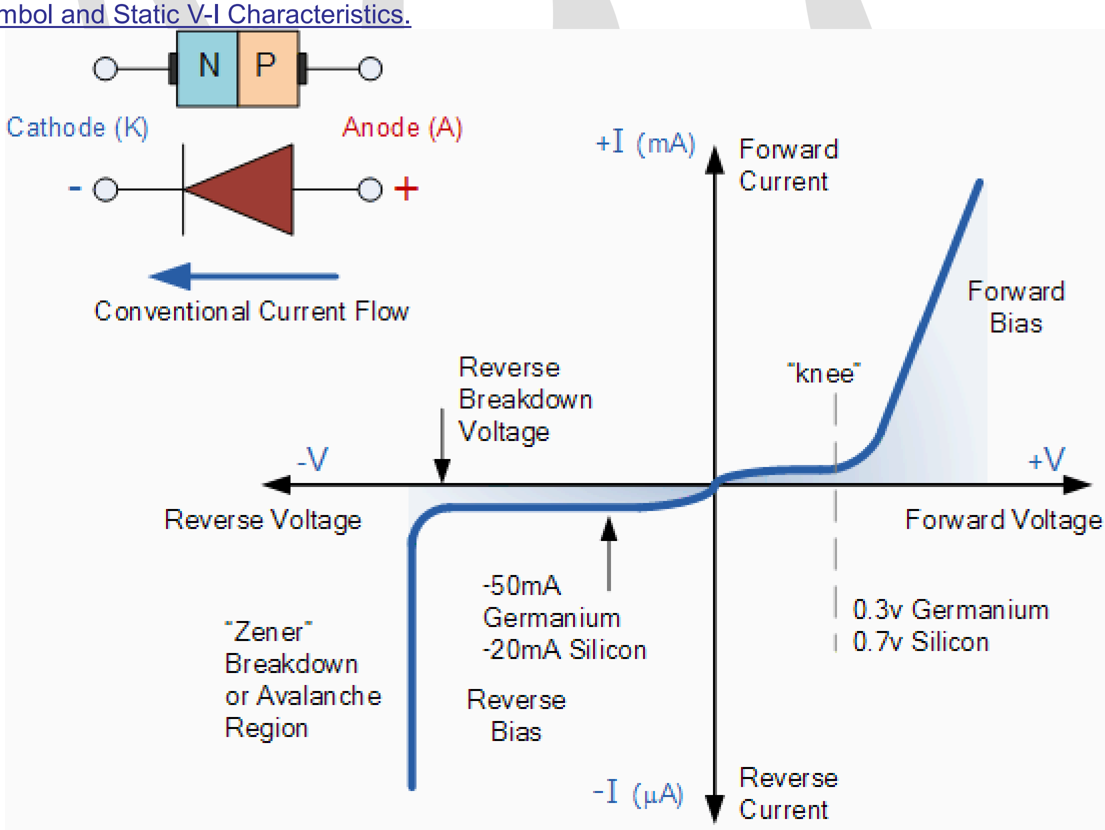
Characteristics	**Ge**	**Si**
Energy gap	0.7 (eV)	1.1 (eV)
Electron mobility (μ_n)	0.39 ($M^2V^{-1}S^{-1}$)	0.135 ($M^2V^{-1}S^{-1}$)
Cotter mobility (μ_p)	0.19 ($M^2V^{-1}S^{-1}$)	0.048 ($M^2V^{-1}S^{-1}$)
Intrinsic current concentration	$n_i = 2.4 \times 10^{19}$ cm^{-3}	$n_i = 1.5 \times 10^{16}$ cm^{-3}
Resistivity	0.46 Ω-m	2300 Ω-m
Potential barrier	0.3 V	0.7 V

(f) Difference between Conductors, Semi-conductors and Insulators

S.No.	Property	Conductors	Semi-conductors	Insulators
1.	Electrical conductivity and its value	Very high 10^{-7} mho/m	Between those of conductors and insulators i.e. 10^{-7} mho/m to 10^{-13} mho/m	Negligible 10^{-13} mho/m
2.	Resistivity and its value	Negligible Less than 10^{-5} Ω-m	Between those of conductors and insulators i.e. 10^{-5} Ω-m to 10^{5} Ω-m	Very high more than 10^{5} Ω-m
3.	Band structure			
4.	Energy gap and its value	Zero or very small	More that in conductors but less than that in insulators e.g. in Ge, ΔE_g =0.72 eV is Si, ΔE_g =1.1 eV in Ga As ΔE_g =1.3 eV	Very large e.g. in diamond ΔE_g = 7 eV
5.	Current carriers and current flow	Due to free electrons and very high	Due to free electrons and holes more than that in insulators	Due to free electrons but negligible.
6.	Number of current carriers (electrons or holes) at ordinary temperature	Very high	very low	negligible

7.	Condition of valence band and conduction band at ordinary temperature	The valence and conduction bands are completely filled or conduction band is some what empty (e.g. in Na)	Valence band in somewhat empty and conduction band is somewhat filled	Valence band is completely filled and conduction band is completely empty.
8.	Behaviour at 0 K	Behaves like a superconductor.	Behaves like an insulator	Behaves like an insulator
9.	Temperature coefficient of resistance (α)	Positive	Negative	Negative
10.	Effects of temperature on conductivity	Conductivity decreases	Conductivity increases	Conductivity increases
11.	On increasing temperature the number of current carriers	Decreases	Increases	Increases
12.	On mixing impurities their resistance	Increases	Decreases	Remains unchanged
13.	Current flow in these takes place	Easily	Very slow	Does not take place
14.	Examples	Cu, Ag, Au, Na, Pt, Hg etc.	Ge, Si, Ga, As etc.	Wood, plastic, mica, diamond, glass etc.

[Junction Diode Symbol and Static V-I Characteristics.]

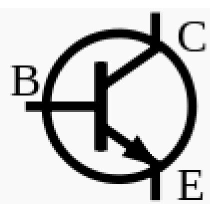


Junction Diode Summary

The PN junction region of a **Junction Diode** has the following important characteristics:

- 1). Semiconductors contain two types of mobile charge carriers, **Holes** and **Electrons**.
- 2). The holes are positively charged while the electrons negatively charged.
- 3). A semiconductor may be doped with donor impurities such as Antimony (N-type doping), so that it contains mobile charges which are primarily electrons.
- 4). A semiconductor may be doped with acceptor impurities such as Boron (P-type doping), so that it contains mobile charges which are mainly holes.
- 5). The junction region itself has no charge carriers and is known as the depletion region.
- 6). The junction (depletion) region has a physical thickness that varies with the applied voltage.
- 7).When a diode is **Zero Biased** no external energy source is applied and a natural **Potential Barrier** is developed across a depletion layer which is approximately 0.5 to 0.7v for silicon diodes and approximately 0.3 of a volt for germanium diodes.
- 8). When a junction diode is **Forward Biased** the thickness of the depletion region reduces and the diode acts like a short circuit allowing full current to flow.
- 9). When a junction diode is **Reverse Biased** the thickness of the depletion region increases and the diode acts like an open circuit blocking any current flow, (only a very small leakage current).

NPN

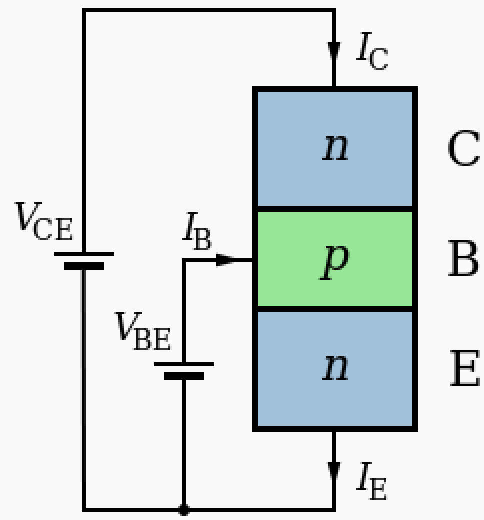


The symbol of an NPN BJT. The symbol is "*n*ot*p*ointing i*n*."

NPN is one of the two types of bipolar transistors, consisting of a layer of P-doped semiconductor (the "base") between two N-doped layers. A small current entering the base is amplified to produce a large collector and emitter current. That is, when there is a positive potential difference measured from the emitter of an NPN transistor to its base (i.e., when the base is **high** relative to the emitter) as well as positive potential difference measured from the base to the collector, the transistor becomes active. In this "on" state, current flows between the collector and emitter of the transistor. Most of the current is carried by electrons moving from emitter to collector as minority carriers in the P-type base region. To allow for greater current and faster operation, most bipolar transistors used today are NPN because electron mobility is higher than hole mobility.

A mnemonic device for the NPN transistor symbol is *n*ot *p*ointing i*n*, based on the arrows in the symbol and the letters in the name.

Active-mode NPN transistors in circuits



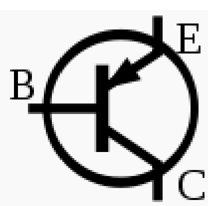
Structure and use of NPN transistor. Arrow according to schematic.

The diagram shows a schematic representation of an NPN transistor connected to two voltage sources. To make the transistor conduct appreciable current (on the order of 1 mA) from C to E, V_{BE} must be above a minimum value sometimes referred to as the **cut-in voltage**. The cut-in voltage is usually about 650 mV for silicon BJTs at room temperature but can be different depending on the type of transistor and its biasing. This applied voltage causes the lower P-N junction to 'turn-on' allowing a flow of electrons from the emitter into the base. In active mode, the electric field existing between base and collector (caused by V_{CE}) will cause the majority of these electrons to cross the upper P-N junction into the collector to form the collector current I_C. The remainder of the electrons recombine with holes, the majority carriers in the base, making a current through the base connection to form the base current, I_B. As shown in the diagram, the emitter current,I_E, is the total transistor current, which is the sum of the other terminal currents, (i.e., $I_E = I_B + I_C$).

In the diagram, the arrows representing current point in the direction ofconventional current – the flow of electrons is in the opposite direction of the arrows because electrons carry negative electric charge. In active mode, the ratio of the collector current to the base current is called the *DC current gain*. This gain is usually 100 or more, but robust circuit designs do not depend on the exact value (for example see op-amp). The value of this gain for DC signals is referred to as h_{FE}, and the value of this gain for small signals is referred to as h_{fe}. That is, when a small change in the currents occurs, and sufficient time has passed for the new condition to reach a steady state h_{fe} is the ratio of the change in collector current to the change in base current. The symbol β is used for both h_{FE} and h_{fe}.[9]

It should also be noted that the emitter current is related to V_{BE} exponentially. At room temperature, an increase in $V_{\mathrm{BE}}$by approximately 60 mV increases the emitter current by a factor of 10. Because the base current is approximately proportional to the collector and emitter currents, they vary in the same way.

PNP

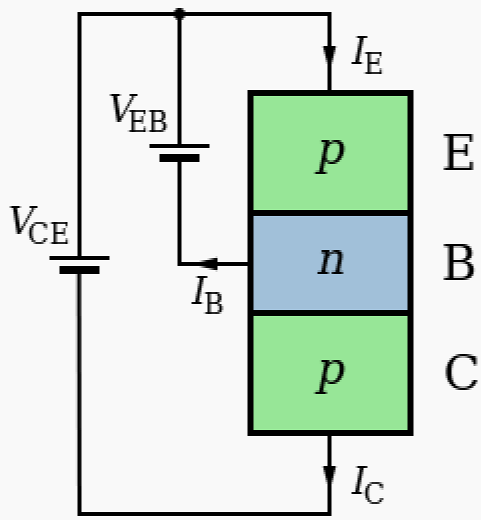


The symbol of a PNP BJT. The symbol "*p*oints i*n*p*r*oudly."

The other type of BJT is the PNP, consisting of a layer of N-doped semiconductor between two layers of P-doped material. A small current leaving the base is amplified in the collector output. That is, a PNP transistor is "on" when its base is pulled **low** relative to the emitter.

The arrows in the NPN and PNP transistor symbols are on the emitter legs and point in the direction of the conventional current flow when the device is in forward active mode.

Active-mode PNP transistors in circuits



Structure and use of PNP transistor.

The diagram shows a schematic representation of a PNP transistor connected to two voltage sources. To make the transistor conduct appreciable current (on the order of 1 mA) from E to C, V_{EB} must be above a minimum value sometimes referred to as the **cut-in voltage**. The cut-in voltage is usually about 650 mV for silicon BJTs at room temperature but can be different depending on the type of transistor and its biasing. This applied voltage causes the upper P-N junction to 'turn-on' allowing a flow of holes from the emitter into the base. In active mode, the electric field existing between the emitter and the collector (caused by V_{CE}) causes the majority of these holes to cross the lower p-n junction into the collector to form the collector current I_{C}. The remainder of the holes recombine with electrons, the majority carriers in the base, making a current through the base connection to form the base current, I_{B}. As shown in the diagram, the emitter current, I_{E}, is the total transistor current, which is the sum of the other terminal currents (i.e., $I_E = I_B + I_C$).

In the diagram, the arrows representing current point in the direction of conventional current – the flow of holes is in the same direction of the arrows because holes carry positive electric charge. In active mode, the ratio of the collector current to the base current is called the *DC current gain*. This gain is usually 100 or more, but robust circuit designs do not depend on the exact value. The value of this gain for DC signals is referred to as h_{FE}, and the value of this gain for AC signals is referred to as h_{fe}. However, when there is no particular frequency range of interest, the symbol β is used.

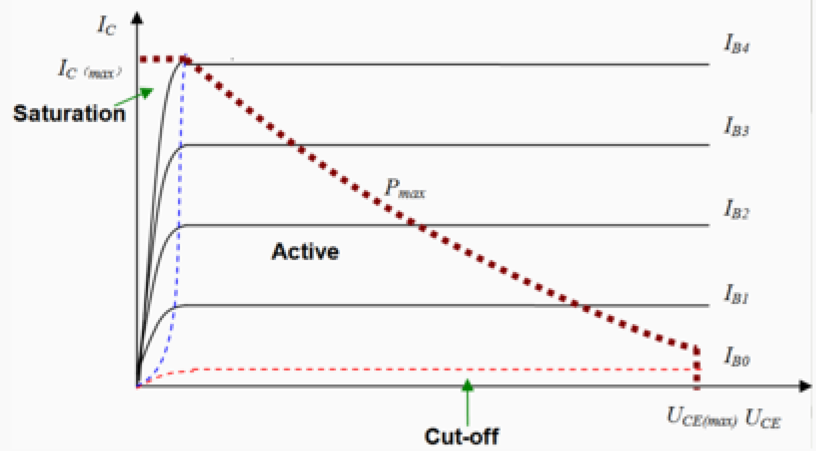
It should also be noted that the emitter current is related to V_{EB} exponentially. At room temperature, an increase in $V_{\mathrm{EB}}$by approximately 60 mV increases the emitter current by a factor of 10. Because the base current is approximately proportional to the collector and emitter currents, they vary in the same way.

Regions of operation

Applied voltages	B-E Junction Bias (NPN)	B-C Junction Bias (NPN)	Mode (NPN)
E < B < C	Forward	Reverse	Forward-active
E < B > C	Forward	Forward	Saturation
E > B < C	Reverse	Reverse	Cut-off
E > B > C	Reverse	Forward	Reverse-active

Applied voltages	B-E Junction Bias (PNP)	B-C Junction Bias (PNP)	Mode (PNP)
E < B < C	Reverse	Forward	Reverse-active
E < B > C	Reverse	Reverse	Cut-off

E > B < C	Forward	Forward	Saturation
E > B > C	Forward	Reverse	Forward-active



The relationship between I_C, U_{CE} and I_B.

Bipolar transistors have five distinct regions of operation, defined by BJT junction biases.

The modes of operation can be described in terms of the applied voltages (this description applies to NPN transistors; polarities are reversed for PNP transistors):

- Forward-active: base higher than emitter, collector higher than base (in this mode the collector current is proportional to base current by β_F).
- Saturation: base higher than emitter, but collector is not higher than base.
- Cut-Off: base lower than emitter, but collector is higher than base. It means the transistor is not letting conventional current go through from collector to emitter.
- Reverse-active: base lower than emitter, collector lower than base: reverse conventional current goes through transistor.

In terms of junction biasing: ('reverse biased base–collector junction' means Vbc < 0 for NPN, opposite for PNP)

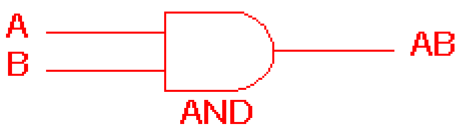
- **Forward-active** (or simply, **active**): The base–emitter junction is forward biased and the base–collector junction is reverse biased. Most bipolar transistors are designed to afford the greatest common-emitter current gain, β_F, in forward-active mode. If this is the case, the collector–emitter current is approximately proportional to the base current, but many times larger, for small base current variations.
- **Reverse-active** (or **inverse-active** or **inverted**): By reversing the biasing conditions of the forward-active region, a bipolar transistor goes into reverse-active mode. In this mode, the emitter and collector regions switch roles. Because most BJTs are designed to maximize current gain in forward-active mode, the β_F in inverted mode is several (2–3 for the ordinary germanium transistor) times smaller. This transistor mode is seldom used, usually being considered only for failsafe conditions and some types of bipolar logic. The reverse bias breakdown voltage to the base may be an order of magnitude lower in this region.
- **Saturation**: With both junctions forward-biased, a BJT is in saturation mode and facilitates high current conduction from the emitter to the collector (or the other direction in the case of NPN, with negatively charged carriers flowing from emitter to collector). This mode corresponds to a logical "on", or a closed switch.
- **Cutoff**: In cutoff, biasing conditions opposite of saturation (both junctions reverse biased) are present. There is very little current, which corresponds to a logical "off", or an open switch.
- **Avalanche breakdown region**

Although these regions are well defined for sufficiently large applied voltage, they overlap somewhat for small (less than a few hundred millivolts) biases. For example, in the typical grounded-emitter configuration of an NPN BJT used as a pulldown switch in digital logic, the "off" state never involves a reverse-biased junction because the base voltage never goes below ground; nevertheless the forward bias is close enough to zero that essentially no current flows, so this end of the forward active region can be regarded as the cutoff region.

Logic gates

Digital systems are said to be constructed by using logic gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the aid of truth tables.

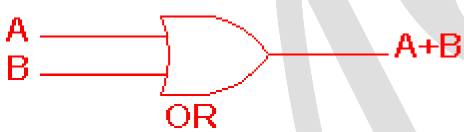
AND gate



2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate is an electronic circuit that gives a **high** output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB

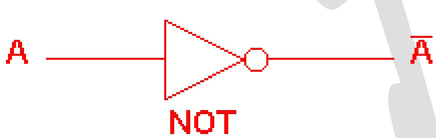
OR gate



2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

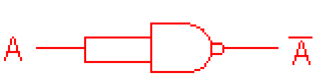
The OR gate is an electronic circuit that gives a high output (1) if **one or more** of its inputs are high. A plus (+) is used to show the OR operation.

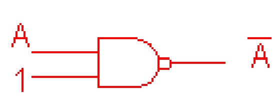
NOT gate



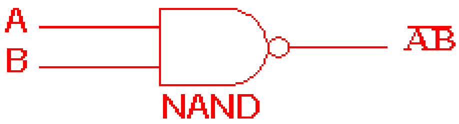
NOT gate	
A	$\overline{A}$
0	1
1	0

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an *inverter*. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs. The diagrams below show two ways that the NAND logic gate can be configured to produce a NOT gate. It can also be done using NOR logic gates in the same way.





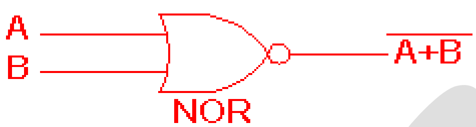
NAND gate



2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

NOR gate

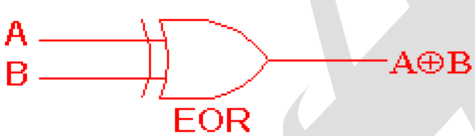


2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high.

The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

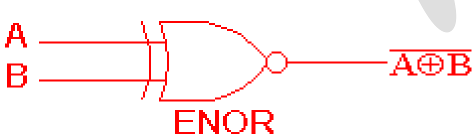
EXOR gate



2 Input EXOR gate		
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

The '**Exclusive-OR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. An encircled plus sign (⊕) is used to show the EOR operation.

EXNOR gate



2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

The '**Exclusive-NOR**' gate circuit does the opposite to the EOR gate. It will give a low output if **either, but not both**, of its two inputs are high. The symbol is an EXOR gate with a small circle on the output. The small circle represents inversion.

The NAND and NOR gates are called *universal functions* since with either one the AND and OR functions and NOT can be generated.

Note:

A function in *sum of products* form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates.

A function in *product of sums* form can be implemented using NOR gates by replacing all AND and OR gates by NOR gates.

Table 1: Logic gate symbols

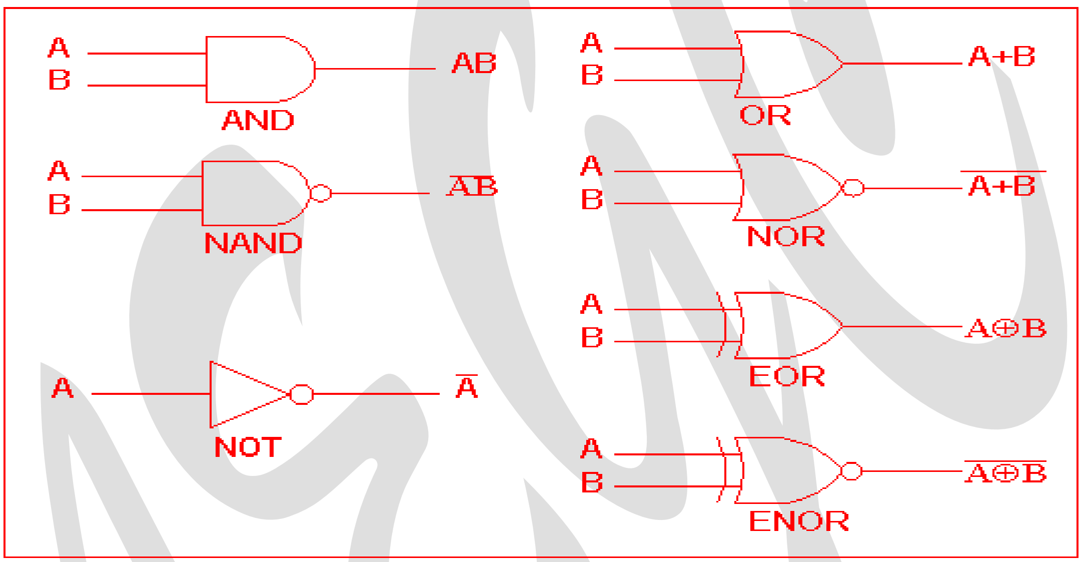


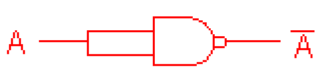
Table 2 is a summary truth table of the input/output combinations for the NOT gate together with all possible input/output combinations for the other gate functions. Also note that a truth table with 'n' inputs has 2^n rows. You can compare the outputs of different gates.

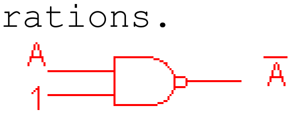
Table 2: Logic gates representation using the Truth table

NOT gate	
A	$\overline{A}$
0	1
1	0

INPUTS		OUTPUTS					
A	B	AND	NAND	OR	NOR	EXOR	EXNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Example:- A NAND gate can be used as a NOT gate using either of the following wiring configurations.





RADIATIONS

X-radiation (composed of **X-rays**) is a form ofelectromagnetic radiation. X-rays have a wavelength in the range of 0.01 to 10 nanometers, corresponding tofrequencies in the range 30 petahertz to 30 exahertz(3×10^{16} Hz to 3×10^{19} Hz) and energies in the range 100eV to 100 keV. The wavelengths are shorter than those of UV rays and longer than of gamma rays. In many languages, X-radiation is called ***Röntgen radiation***, afterWilhelm Röntgen